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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
FAN, CHIEH M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/764,680	WRIGHT, ANDREW S.	
	Examiner	Art Unit	
	Chieh M Fan	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03292001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 3/29/2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. The examiner is able to obtain the copies of the U.S. and foreign patents listed thereon. However, the references listed under "other documents" have not been considered.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-6 and 20-29 are objected to because of the following informalities:

Regarding claim 1, "a digital error signal" in line 6 should be changed to --- the digital error signal" and "a desired output signal" in lines 13-14 should be changed to --- the desired output signal --- since such limitations have been recited in the preamble.

Regarding claim 6, "a desired output signal" in line 2 should be changed to --- the desired output signal ---.

Regarding claim 20, "subtracting the second signal" in line 9 should be changed to --- subtracting the delayed second signal ---.

Regarding claim 25, "subtracting the second signal" in line 9 should be changed to --- subtracting the delayed second signal ---.

Regarding claim 26, "a second digital-to-analog converter" is recited in line 15, but a first digital-to-analog converter is never mentioned.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 7-19, 22, 23, 26-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 7, the claimed limitation "sampling an output of the power amplifier" in line 9 has no support in the specification. In general, it is known in the art, the process of sampling involves taking the values of an analog or continuous signal periodically to generate discrete values. As shown in Figs. 3 and 4, there is clearly no sampling process.

Regarding claim 9, claim 9 also recites "receiving a sample of the output signal of the transmitter" in line 4 and is therefore rejected for the reason applied to claim 7 above.

Regarding claim 19, claim 19 also recites "receiving a sample of the output signal of the transmitter" in line 4 and is therefore rejected for the reason applied to claim 7 above. Further, claim 19 recites the step of converting the input signal to an analog signal followed by the step of delaying the analog input signal. These two steps are exactly opposite to the teaching of the specification (see 314 and 316 of the Fig. 3).

Regarding claims 22 and 23, the applicant is invited to indicate which portion of the specification supports the claimed limitations. Particularly, it appears that the FIR 314 in Fig. 3 performs the claimed limitation on the second signal, i.e., the delayed signal, not the first signal.

Regarding claim 26, claim 26 also recites "provides a sample of the amplified modulated carrier" in line 10 and is therefore rejected for the reason applied to claim 7 above.

Regarding claim 30, claim 30 also recites "convert a sample of the RF output signal" in lines 11-12 and is therefore rejected for the reason applied to claim 7 above.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the first modified signal" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (U.S. Patent No. 4,291,277, listed in the IDS filed 3/29/01, "Davis" hereinafter) in view of Flugstad et al. (U.S. Patent No. 4,810,977, "Flugstad" hereinafter).

Davis teaches a power amplifier system in which a digital input transmission signal is adaptively predistorted to compensate for non-linearities in an amplification process based on a difference between a desired and an observed amplifier output, a method of generating a digital error signal that accurately represents said difference, comprising:

adaptively processing the digital input transmission signal (21 in fig. 4) at least partially in response to a digital error signal to generate a modified signal that complements non-linearities resulting from the amplification process (34 in Fig. 4);

converting the modified signal to analog form to produce an analog modified signal, which is related signal that is amplified by the amplification process (23I, 23Q in Fig. 4);

down-converting a radio frequency (RF) signal that represents an actual output of the amplifier system to generate a feedback signal (33, 29 in Fig. 4);

processing the digital input transmission signal to provide a desired output signal (13 in Fig. 4);

converting the desired output signal to analog form to produce an analog delayed signal (15I, 15Q in Fig. 4);

taking a difference between the feedback signal and the desired output signal to generate an analog error signal (17I, 17Q in Fig. 4); and

using an analog-to-digital converter to convert the error signal to digital form to produce the digital error signal (38I, 38Q in Fig. 4).

Davis does not teach the step of scaling the analog error signal to produce a scaled error signal that substantially corresponds to a range of an analog-to-digital converter (ADC).

However, it is well known in the art that the input to an ADC needs to be limited within the dynamic range of the ADC so as to provide accurate results. Flugstad teaches scaling the input to an ADC to permit the use of the full range of ADC. If the ADC is not utilized over its full range, accuracy and resolution is lost (col. 4, lines 6-9). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to scale the outputs 18I, 18Q of the summation circuit 17I, 17Q of Davis before they are input to the ADC's 38I, 38Q, so as to provide accurate results.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (U.S. Patent No. 4,291,277, listed in the IDS filed 3/29/01, "Davis" hereinafter) in view of Flugstad et al. (U.S. Patent No. 4,810,977, "Flugstad" hereinafter) as applied to claim 1 above, and further in view of Ichiyoshi (U.S. Patent No. 5,699,383).

Davis in view of Flugstad teaches the claimed invention, but does not specifically teach delaying the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal.

However, such delaying is inherent and explicitly required for the comparators (or summation circuits) 17I and 17Q to make proper comparison, otherwise erroneous

comparison results will be generated due to misalignment. In the same field of endeavor, Ichiyoshi teaches such delay (27 in Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to delay the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal, since such delay is explicitly required to provide a proper comparison result.

11. Claims 7-12, 19, 20, 24-26 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (U.S. Patent No. 4,291,277, listed in the IDS filed 3/29/01, "Davis" hereinafter) in view of Ichiyoshi (U.S. Patent No. 5,699,383).

Regarding claim 7, Davis teaches a method of transmitting a radio frequency (RF) power signal, the method comprising:

receiving an input signal (10, 12 in Fig. 4);

predistorting the input signal (21 in Fig. 4), where the predistortion compensates for at least part of an intrinsic distortion of a power amplifier (34 in Fig. 4);

up-converting the predistorted input signal such that a carrier wave is modulated with the predistorted input signal (26, 32 in Fig. 4);

amplifying the modulated carrier wave with the power amplifier (34 in Fig. 4);

receiving an output of the power amplifier (36 in Fig. 4);

down-converting the signal of the output of the power amplifier to an intermediate frequency (33, 29 in Fig. 4);

combining the delayed input signal with the down-converted sample such that an amplitude of the combined signal is less than an amplitude of the down-converted sample (17I, 17Q in Fig. 4);

converting the combined signal from analog to digital (38I, 38Q in Fig. 4); and

receiving the digital combined signal and revising the predistorting of the input signal in response to the digital combined signal such as to reduce a distortion in the output of the power amplifier (20I, 20Q in Fig. 4).

Davis does not particularly teach the step of delaying the input signal such that a content of the input signal is substantially time aligned with the content of the down-converted sample of the output of the power amplifier. However, such step of delaying is inherent and explicitly required for the comparators (or summation circuits) 17I and 17Q to make proper comparison, otherwise erroneous comparison results will be generated due to misalignment. In the same field of endeavor, Ichiyoshi teaches such delaying (27 in Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to delay the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal, since such delay is explicitly required to provide a proper comparison result.

Regarding claim 8, the combining of the delayed input signal with the down-converted sample substantially eliminates a main signal component of the down-converted sample from the combined signal (col. 6, lines 18-21, that is, the outputs of

the summation circuits 17I and 17Q are the variation in the AM/AM and AM/PM conversion character of the power amplifier).

Regarding claim 9, Davis teaches a method of generating an error signal that can be used to reduce distortion in a radio frequency (RF) output signal of an RF transmitter, the method comprising:

Receiving an output signal of the transmitter (36 in Fig. 4);

down-converting the signal of the output signal from an RF signal to a down-converted signal (33, 29 in Fig. 4);

receiving an input signal of the transmitter 910, 12 in Fig. 4), where the input signal is digital;

converting, from digital to analog, a delayed input signal to the analog delayed input signal (15I, 15Q in Fig. 4);

combining the down-converted signal with the analog delayed input signal to produce a modified down-converted signal such that an amplitude of the modified down-converted signal is reduced relative to an amplitude of the down-converted signal (17I, 17Q in Fig. 4); and

converting the modified down-converted signal, from analog to digital, to produce the error signal (38I, 38Q in Fig. 4).

Davis does not particularly teach the step of delaying the input signal to produce a delayed input signal to approximately time align an analog delayed input signal with the down-converted signal. However, such step of delaying is inherent and explicitly required for the comparators (or summation circuits) 17I and 17Q to make proper

comparison, otherwise erroneous comparison results will be generated due to misalignment. In the same field of endeavor, Ichiyoshi teaches such delaying (27 in Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to delay the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal, since such delay is explicitly required to provide a proper comparison result.

Regarding claim 10, wherein down-converting the signal of the output signal from the RF signal to the down-converted signal comprises down-converting the signal to complex baseband (30I, 30Q in Fig. 4).

Regarding claim 11, wherein down-converting the signal of the output signal from the RF signal to the down-converted signal comprises down-converting the signal to an Intermediate Frequency (see output of 33 in Fig. 4).

Regarding claim 12, wherein combining the down-converted signal with the analog delayed input signal further comprises subtracting the analog delayed input signal from the down-converted signal (17I, 17Q in Fig. 4, col. 4, lines 61-65).

Regarding claims 19 and 24, Davis teaches a method of generating an error signal that can be used to reduce distortion in a radio frequency (RF) output signal of an RF transmitter, the method comprising:

receiving a signal of the output signal of the transmitter (36 in Fig. 4);

down-converting the signal of the output signal from an RF signal to a down-converted signal (33, 29 in Fig. 4);

receiving an input signal of the transmitter, where the input signal is digital (10, 12 in Fig. 4);

converting, from digital to analog, the input signal to an analog input signal (15I, 15Q in Fig. 4);

combining the down-converted signal with a delayed analog input signal to produce a modified down-converted signal such that an amplitude of the modified down-converted signal is reduced relative to an amplitude of the down-converted signal (17I, 17Q in Fig. 4); and

converting the modified down-converted signal, from analog to digital, to produce the error signal (38I, 38Q in Fig. 4).

Davis does not particularly teach the step of delaying the input signal to produce a delayed input signal to approximately time align an analog delayed input signal with the down-converted signal. However, such step of delaying is inherent and explicitly required for the comparators (or summation circuits) 17I and 17Q to make proper comparison, otherwise erroneous comparison results will be generated due to misalignment. In the same field of endeavor, Ichiyoshi teaches such delaying (27 in Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to delay the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal, since such delay is explicitly required to provide a proper comparison result.

Regarding claims 20, 24 and 25, Davis teaches a method of responsively filtering a first component from a first signal to efficiently utilize an input range of an analog-to-digital converter used to detect and measure a second component of the first signal, the method comprising:

receiving the first signal (30I, 30Q in Fig. 4);

receiving a second signal, where the second signal is related to the first component of the first signal (15I, 15Q in Fig. 4);

delaying the second signal to align the second signal with the first component of the first signal;

subtracting the second signal from the first signal to generate an error signal (17I, 17Q in Fig. 4, col. 4, lines 61-65); and

applying the error signal to the analog-to-digital converter (38I, 38Q in Fig. 4).

Davis does not particularly teach the step of delaying the second signal to align the second signal with the first component of the first signal. However, such step of delaying is inherent and explicitly required for the comparators (or summation circuits) 17I and 17Q to make proper comparison, otherwise erroneous comparison results will be generated due to misalignment. In the same field of endeavor, Ichiyoshi teaches such delaying (27 in Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to delay the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal, since such delay is explicitly required to provide a proper comparison result.

Regarding claim 26, Davis teaches radio frequency (RF) transmitter with adaptive predistortion comprising:

a predistortion circuit (21 in Fig. 4) that predistorts an input signal to a predistorted input signal in response to maintained coefficients in a predistortion kernel, where the predistortion is substantially complementary to an intrinsic distortion in an RF power amplifier (34 in Fig. 4);

an RF up-converter (26, 32 in Fig. 4), which produces a modulated a carrier wave from the predistorted input signal;

the RF power amplifier (34 in Fig. 4), which amplifies the modulated carrier wave;

a coupler (35 in Fig. 4), which provides a signal of the amplified modulated carrier;

an RF down-converter (33, 29 in Fig. 4), which converts the signal of the amplified modulated carrier wave to a down-converted signal;

a digital-to-analog converter (15I, 15Q in Fig. 4) that converts a delayed input signal to an analog delayed input signal;

a summing node (17I, 17Q in Fig. 4) adapted to combine the analog delayed input signal with the down-converted signal to generate a summed Output such that the analog delayed input signal and the down-converted signal at least partially destructively interfere;

an analog-to-digital converter (38I, 38Q in Fig. 4) that converts the slummed output to a digital summed output; and

an adaptive control processing and compensation estimator circuit (19I, 19Q in Fig. 4) that monitors the digital summed output and provides updates to the predistortion circuit such that the predistortion of the input signal remains substantially complementary to the intrinsic distortion of the RF power amplifier.

Davis does not particularly teach a delay circuit for delaying the input signal to produce the delayed input signal. However, such delay circuit is inherent and explicitly required for the comparators (or summation circuits) 17I and 17Q to make proper comparison, otherwise erroneous comparison results will be generated due to misalignment. In the same field of endeavor, Ichiyoshi teaches a delay circuit (27 in Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to delay the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal, since such delay is explicitly required to provide a proper comparison result.

Regarding claim 32, Davis teaches a circuit that filters a first component (the signal to be transmitted in Fig. 4) from a first signal (30I, 30Q in Fig. 4) to efficiently utilize an input range of an analog-to-digital converter (38I, 38Q in Fig. 4) used to detect and measure a second component (distortion introduced by power amplifier 34 in Fig. 4) of the first signal, the circuit comprising:

a conversion circuit (15I, 15Q in Fig. 4) adapted to convert a delayed second signal (14I, 14Q in Fig. 4) from digital to analog form; and

a comparison circuit (17I, 17Q in Fig. 4) adapted to combine the analog form of the delayed second signal with the first signal such that the presence of the first component is diminished in an output of the comparison circuit (col. 6, lines 18-21, the outputs of the summation circuits 17I and 17Q are only the variation in the AM/AM and AM/PM conversion character of the power amplifier, i.e., the distortion introduced by the power amplifier 34).

Davis does not particularly teach a delay circuit adapted to delay a second signal to a delayed second signal such that an analog form of the delayed second signal aligns with the first component of the first signal. However, such delay circuit is inherently and explicitly required for the comparators (or summation circuits) 17I and 17Q to make proper comparison, otherwise erroneous comparison results will be generated due to misalignment. In the same field of endeavor, Ichiyoshi teaches a delay circuit (27 in Fig. 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to delay the desired signal relative to the input transmission signal such that the desired signal is substantially time aligned with the feedback signal, since such delay is explicitly required to provide a proper comparison result.

12. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (U.S. Patent No. 4,291,277, listed in the IDS filed 3/29/01, "Davis" hereinafter) in view of Ichiyoshi (U.S. Patent No. 5,699,383) as applied to claim 20 above, and further in view of Flugstad et al. (U.S. Patent No. 4,810,977, "Flugstad" hereinafter).

Davis in view of Ichiyoshi teaches the claimed invention, but does not teach the step of adjusting a relative amplitude of the error signal versus an input range of the analog-to-digital converter such that the error signal approximately conforms to the input range. However, it is well known in the art that the input to an ADC needs to be limited within the dynamic range of the ADC so as to provide accurate results. Flugstad teaches scaling the input to an ADC to permit the use of the full range of ADC. If the ADC is not utilized over its full range, accuracy and resolution is lost (col. 4, lines 6-9). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to scale the outputs 18I, 18Q of the summation circuit 17I, 17Q of Davis before they are input to the ADC's 38I, 38Q, so as to provide accurate results.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (703) 305-0198. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703) 305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Chieh M Fan
Primary Examiner
Art Unit 2634

cmf
August 22, 2004